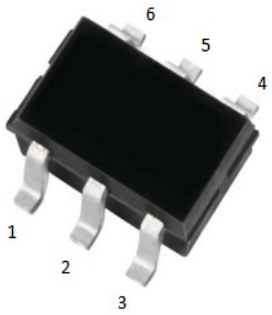
# 2N7002KDW

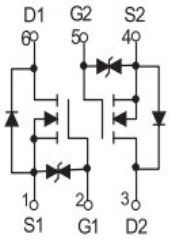
**N-Channel SMD MOSFET**

## 1. Features

- High density cell design for ultra low on-resistance
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability
- ESD protected

SOT-363




## 2. Mechanical Data

- Case:Molded Plastic,SOT-363 .
- Epoxy:UL 94V-0 rate flame retardant.
- Terminals:Plated Leads Solderable per MIL-STD-750,Method-2026.
- Marking:.72K
- Mounting Position : Any.

## 3. Maximum Ratings

Electrical Characteristics Rating at 25℃ ambient temperature unless otherwise specified.

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $I_D$ | 340 | mA |
| Power Dissipation | $P_D$ | 150 | mW |
| Thermal Resistance from Junction to Ambient | $R_{\theta JA}$ | 833 | ℃/W |
| Junction Temperature | $T_j$ | -55～+150 | ℃ |
| Storage Temperature | $T_{stg}$ | -55～+150 | ℃ |

## 4. Electrical Characteristics($T_A$=25℃ unless otherwise noted)

| Characteristics | Symbol | Condition | Min | TYP | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V,$I_D$ =250μA | 60 | - | - | V |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ =48V,$V_{GS}$ = 0V | - | - | 1 | μA |
| Gate-body leakage current | $I_{GSS}$ | $V_{GS}$ =±20V, $V_{DS}$ = 0V | - | - | ±10 | μA |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ =1mA | 1.0 | - | 2.5 | V |
| Drain-source on-resistance(1) | $R_{DS(on)}$ | $V_{GS}$ =10V, $I_D$ =500A | - | 0.9 | 5 | Ω |
| | | $V_{GS}$ =4.5V, $I_D$ =200A | - | 1.1 | 5.3 | |
| Input Capacitance(2) | $C_{iss}$ | VDS =10V,VGS =0V,f =1MHz | - | - | 40 | pF |
| Output Capacitance(2) | $C_{oss}$ | | - | - | 30 | |
| Reverse Transfer Capacitance(2) | $C_{rss}$ | | - | - | 10 | |
| Turn-on delay time(2) | $t_{d(on)}$ | VDD=50V,VGS=10V, RL=250Ω,RGEN=50Ω | - | - | 10 | ns |
| Turn-off delay time(2) | $t_{d(off)}$ | | - | - | 15 | |
| Diode Forward voltage | $V_{SD}$ | $V_{GS}$ =0V, $I_S$=0.3A | - | - | 1.5 | V |

Notes：

1. Pulse Test: Pulse Width < 300μs, Duty Cycle ≤2%.
2. Guaranteed by design, not subject to production testing.

## 5. Rating And Characteristic Curves

Fig.1 Output Characteristics

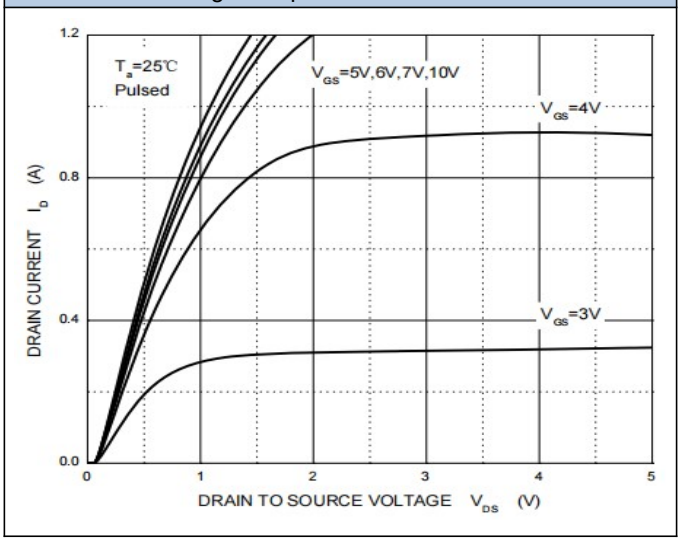



Fig.2 Transfer Characteristics

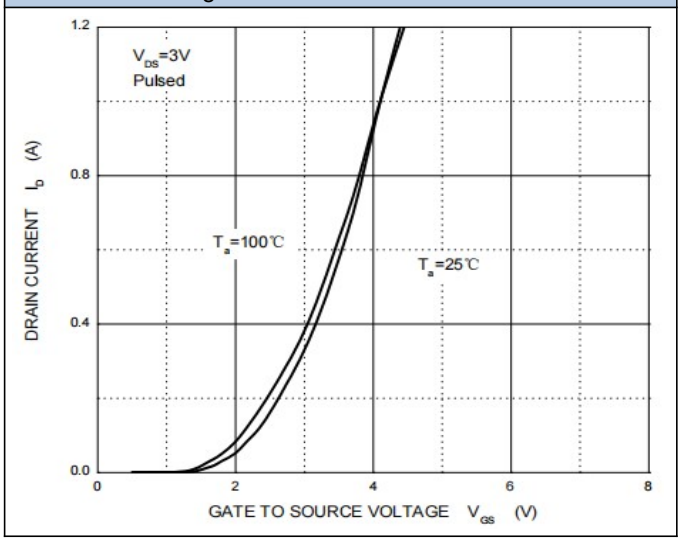



Fig.3 $R_{DS(ON)}$ - $I_D$

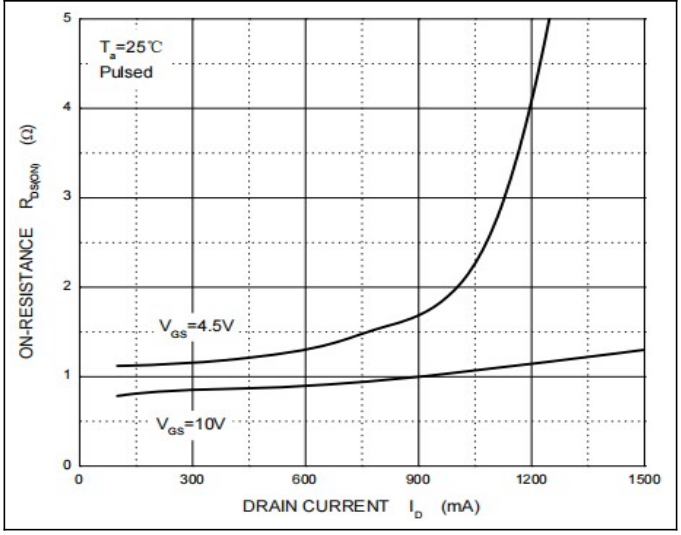



Fig.4 $R_{DS(ON)}$ - $V_{GS}$

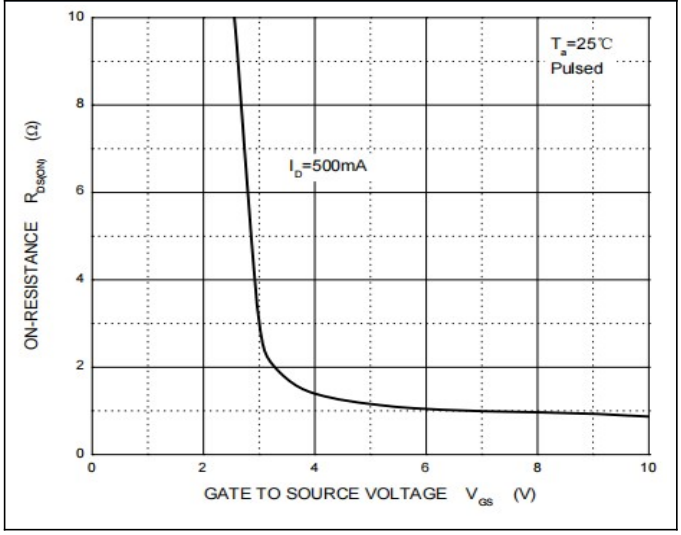



Fig.5 $I_S$ - $V_{SD}$

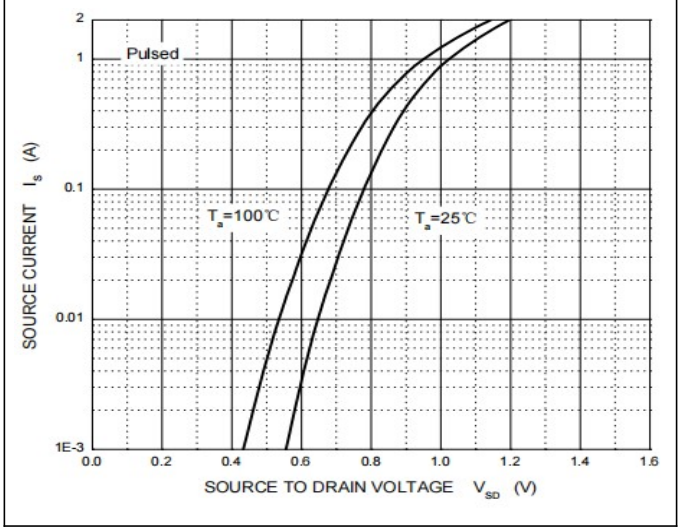
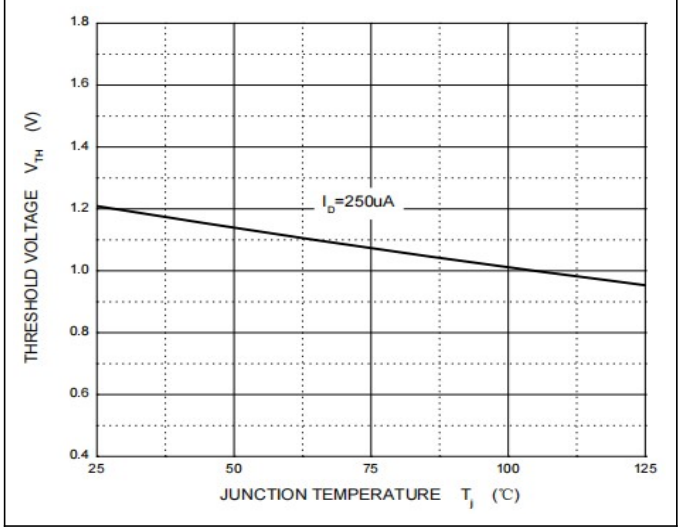
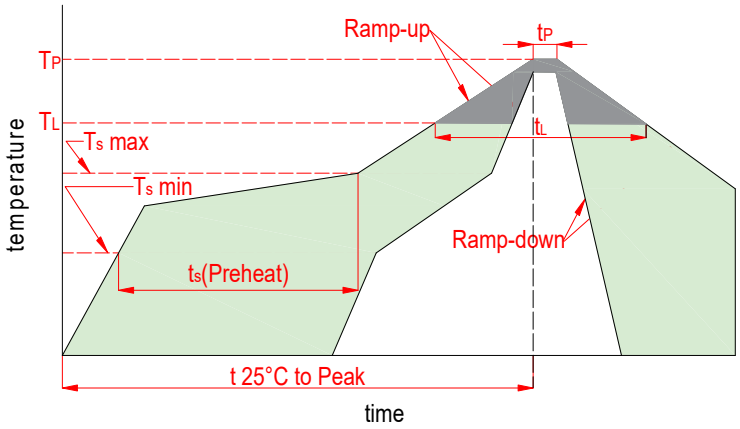



Fig.6 Threshold Voltage

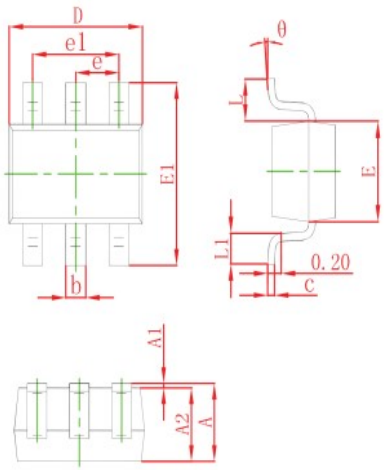


## 6. Soldering Parameters



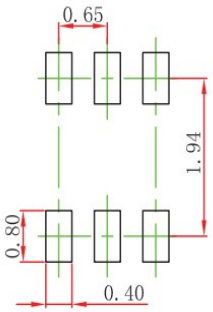

| Reflow Condition | | Lead-free |
|---|---|---|
| Pre Heat | Temp. min($T_s$(min)) | 150℃ |
| | Temp. max($T_s$(min)) | 200℃ |
| | Time(min to max)($t_s$) | 60~120s |
| Aver. ramp up rate(Liquidus Temp.)($T_L$)to peak | | 3℃/s max |
| $T_S$(max) to $T_L$-Ramp-up Rate | | 3℃/s max |
| Reflow | Temp.($T_L$)(Liquidus) | 217℃ |
| | Temp.($t_L$)(Liquidus) | 60~150s |
| Peak Temp.($T_P$) | | $260^{+0/-5}$℃ |
| Time within actual peak Temp.($t_p$) | | 30s max |
| Ramp-down Rate | | 6℃/s max |
| Time 25℃ to peak Tempe.($T_p$) | | 8 minutes max |
| Do not exceed | | 260℃ |

## 7. Dimensions

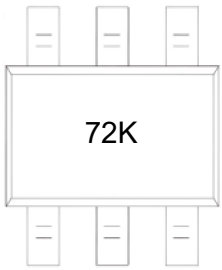



| Dimensions | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.035 | 0.043 | 0.900 | 1.100 |
| A1 | 0.000 | 0.004 | 0.000 | 0.100 |
| A2 | 0.035 | 0.039 | 0.900 | 1.000 |
| b | 0.006 | 0.014 | 0.150 | 0.350 |
| c | 0.003 | 0.006 | 0.080 | 0.150 |
| D | 0.079 | 0.087 | 2.000 | 2.200 |
| E | 0.045 | 0.053 | 1.150 | 1.350 |
| E1 | 0.085 | 0.096 | 2.150 | 2.450 |
| e1 | 0.047 | 0.055 | 1.200 | 1.400 |
| L1 | 0.010 | 0.018 | 0.260 | 0.460 |

Mounting PAD Layout




## 8. Part Marking System




## 9. Package Information

| Package | Part Number | Tape Width(mm) | Quantity(pcs) |
|---|---|---|---|
| SOT-363 | 2N7002KDW | 8 | 3000 |

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